Claims

What is claimed is:

1. A semiconductor integrated circuit, comprising:

a first amplifier circuit which receives a first potential and then supplies a current to an output terminal;

a second amplifier circuit which receives a second potential and then absorbs a current from the output terminal; and

a control circuit which controls the second amplifier circuit so that the second amplifier circuit starts operating subsequent to a predetermined period of time that elapses after the first amplifier circuit is activated.

2. The semiconductor integrated circuit according to claim 1, further comprising a potential generating circuit which generates the first potential and the second potential so as to make the first potential higher than the second potential.

3. The semiconductor integrated circuit according to claim 1, wherein:

the first amplifier circuit comprises a first differential amplifier and a p-channel transistor of an output stage; and

the second amplifier circuit comprises a second differential amplifier and an n-channel transistor of the output stage.

4. The semiconductor integrated circuit according to claim 3, wherein:

the first amplifier circuit further comprises a first transistor which makes the p-channel transistor of the output stage cut off according to a first control signal in a first mode; and

the second amplifier circuit further comprises a first transistor which makes the n-channel transistor of the output stage cut off according to a second control signal in the first mode and a second mode.

5. The semiconductor integrated circuit according to claim 4, wherein:

the first amplifier circuit further comprises a second transistor which supplies a current to two transistors forming a differential pair of the

first differential amplifier according to a first control signal in the second mode and a third mode; and

the second amplifier circuit further comprises a second transistor which supplies a current to two transistors forming a differential pair of the second differential amplifier according to a second control signal in the third mode.

6. The semiconductor integrated circuit according to claim 1, wherein the control circuit, by counting a clock signal, makes a state of a second control signal supplied to the second amplifier circuit change subsequent to a predetermined period of time that elapses after a state of a first control signal supplied to the first amplifier circuit changes.